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POWER ELECTRONICS

STUDENT MANUAL

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1. OPEN-LOOP BUCK CONVERTER

A buck converter is a step-down DC to DC switch-mode converter. It uses two switches (a transistor and a diode) and a second-order low-pass filter (an inductor and a capacitor). The goal of this exercise is to design a buck converter supplying 48 V to a resistive load. Solve the following questions:

1) Find the inductor and capacitor values that meets the design specifications.
2) Complete the following table taking into consideration that the load resistor is changing. The steady-state measures D, Po, Imin and To represent transistor duty cycle, output power, minimum inductor current and time interval in which the inductor current is zero in a switching period, respectively.

R (ohm)	Vo (V)	Vo/Vi	D	Po (W)	Imin (A)	To (us)
4.6	48					
9.2	48					
46	48					
92	48					

3) Discuss briefly the results obtained in the previous question. Why the duty cycle decreases for high values of the load resistor?
4) A synchronous buck converter is a buck converter in which the diode is replaced with a transistor. Repeat question 2 using a synchronous buck converter.
5) Compare the results obtained in questions 2 and 4.

DESIGN SPECIFICATIONS

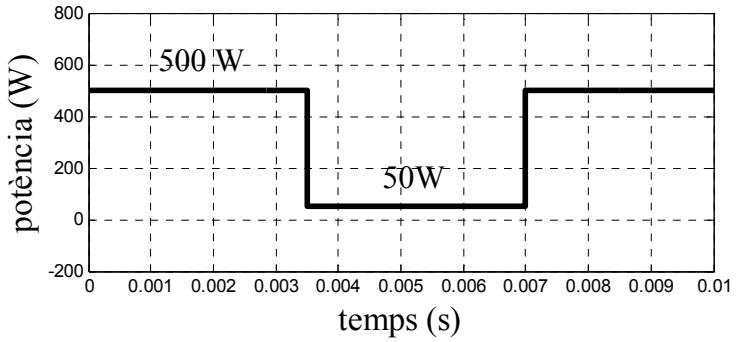
Parameter	Value	Unit
Input voltage, Vi	300	V
Output voltage, Vo	48	V
Maximum output power, Pomax	500	W
Switching frequency, fs	100	kHz
Inductor current ripple, ΔI_L	40	%
Capacitor voltage ripple, ΔV_C	1	%

Note: Ripples are defined as (max value – min value) / average value.

2. CLOSED-LOOP BUCK CONVERTER

The goal of this exercise is to design the closed-loop control of a buck converter. Also the performance of this system will be evaluated. Use the components (L and C) and the design specifications of exercise 2, and solve the following questions:

1) Propose a closed-loop control system which ensures that the DC output voltage is 48 V at steady state.
2) Modify the control system to obtain a soft start in the output voltage.
3) Add a sinusoidal disturbance to the input voltage (60 Vpeak, 1kHz). What is the effect of this disturbance on the output voltage?
4) Simulate a variable load with the power consumption profile shown in the figure below. What is the effect of this load on the output voltage?



5) Complete the following table with the results obtained by different working groups. The transient response measures ΔVo and ts denote maximum output voltage deviation and settling time during load changes, respectively. What is the best result? Why?

group	$\Delta Vo_{500\rightarrow 50}$ (V)	$ts_{500\rightarrow 50}$ (us)	$\Delta Vo_{50\rightarrow 500}$ (V)	$ts_{50\rightarrow 500}$ (us)
1				
2				
3				
4				
5				